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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/721,099	11/26/2003	Toshihiko Okamura	Q78646	6194

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EXAMINER	
RIZK, SAMIR WADIE	
ART UNIT	**PAPER NUMBER**
2133	

DATE MAILED: 06/29/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/721,099	OKAMURA ET AL.	
	Examiner	Art Unit	
	Sam Rizk	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/26/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTIONS

- Claims 1-22 have been submitted for examination
- Claims 1-22 have been rejected

Specification

1. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-22 are rejected under 35 U.S.C. 102(e) as being anticipated by Richardson et al. US publication no. 2005/0278606 (Hereinafter Richardson).

3. In regard to claim 1, Richardson teaches:

- An error correcting code decoding device based on Message-passing decoding on a Low-Density Parity-check Code, comprising:

(Note: Abstract in Richardson)

- a plurality of memory means for storing a received value and a message generated during said decoding;

(Note: Figure 9, reference signs (906),(910) and (912) in Richardson)

- a plurality of variable node function means in said decoding;

(Note: Figure 9, reference sign (908) in Richardson)

- a plurality of check node function means in said decoding;

(Note: Figure 9, reference sign (908) in Richardson)

- a plurality of address generation means for generating an address of said memory means; and

(Note: Figure 9, reference sign (904) and section [0109], line 17 in Richardson)

- a plurality of shuffle network means for determining a connection between said variable node function means and said check node function means;

(note: section [0107] in Richardson)

- wherein said address generation means generates said address on the basis of a plurality of permutations and each of said shuffle network means being connected to some of said variable node function means said connection being determined on the basis of a plurality of permutations. a change of said permutations in said address generation means and a change of said permutations in said shuffle network means being performed in the same cycle in a decoding process.

(Note: section [0109] in Richardson)

4. In regard to claim 2, Richardson teaches:

- The error correcting code decoding device according to claim 1 wherein said address generation means singly generates an address for all of said memory means; and
- wherein said shuffle network means is singly connected to all of said variable node function means.

(Note: Figure 9, reference sign (904) in Richardson)

5. In regard to claim 3, Richardson teaches:

- The error correcting code decoding device according to claim 1.
- wherein said memory means stores said message with a sum thereof.

(Note: section [0120] in Richardson)

6. In regard to claim 4, Richardson teaches:

- The error correcting code decoding device according to claim 1.
- wherein said address generation means is provided as a counter.

(Note: section [0107] in Richardson)

7. In regard to claim 5, Richardson teaches:

- The error correcting code decoding device according to claim 1.
- wherein a permutation by said shuffle network means is determined on the basis of a Galois field calculation.

(Note: section [0025], line (22) in Richardson)

8. In regard to claim 6, Richardson teaches:

- The error correcting code decoding device according to claim 1

- wherein said decoding corrects a message of an output from said check node function means by multiplying it by a coefficient less than 1 on the basis of the min-sum algorithm.

(Note: section [0120] in Richardson)

9. In regard to claim 7, Richardson teaches:

- The error correcting code decoding device according to claim 1.
- wherein in said decoding, said check node function means holds the minimum value of the absolute value of an input message and an index thereof, and the second minimum value of the input message and information whether the input message is positive or negative on the basis of the min-sum algorithm.

(Note: Figure 17, reference sign (1709) in Richardson)

10. In regard to claim 8, Richardson teaches:

- The error correcting code decoding device according to claim 1.
- wherein decoding on a different code is dealt with by changing only said address generation means.

(Note: section [0042], lines (12-16) in Richardson)

11. In regard to claim 9, Richardson teaches:

- The error correcting code decoding device according to claim 1
- wherein decoding on an uniform Low-Density Parity-check Code is implemented by providing a function to always send a message that the output has a codeword bit with an extremely high probability of 0 to

a set of said variable node function means corresponding to one of said address generation means and said shuffle network means.

(Note: Figure 1 or 2 in Richardson)

12. Claim 10 is rejected for the same reasons as per claim 1.

13. Claim 11 is rejected for the same reasons as per claim 3.

14. Claim 12 is rejected for the same reasons as per claim 5.

15. Claim 13 is rejected for the same reasons as per claim 6.

16. In regard to claim 14, Richardson teaches:

- The program according to claim 10,
- wherein in said decoding, said check node function means holds the minimum value of the absolute value of an input message and an index thereof, and the second minimum value of the input message and information whether the input message is positive or negative on the basis of the min-sum algorithm.

(Note: section [0033] in Richardson)

17. Claim 15 is rejected for the same reasons as per claim 8.

18. Claim 16 is rejected for the same reasons as per claim 9.

19. In regard to claim 17, Richardson teaches:

- An error correcting code decoding method on the basis of Message-passing decoding on a Low=Density Parity-check Code, comprising the steps of:

- generating an address of a memory storing a received value and a message generated during said decoding on the basis of a plurality of permutations;

(Note: section [0109] in Richardson)

- connecting a plurality of variable node function in said decoding and a plurality of check node function in said decoding on the basis of a permutation changed in the same cycle as that of said address generation means.

(note: sections [0107] and [0109] in Richardson)

20. Claim 18 is rejected for the same reasons as per claim 3.

21. Claim 19 is rejected for the same reasons as per claim 5.

22. Claim 20 is rejected for the same reasons as per claim 6.

23. Claim 21 is rejected for the same reasons as per claim 7.

24. Claim 22 is rejected for the same reasons as per claim 8.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- Richardson et al. US publication no. 2005/0257124 teaches node processors for use in parity check decoders.

- Tran et al US publication no. 2006/0085720 teaches message passing memory and barrel shifter arrangement in LDPC (low density parity check) decoder supporting multiple LDPC codes.
- Tran et al. US publication 2005/0268206 teaches common circuitry supporting both bit node and check node processing in LDPC decoder.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Rizk whose telephone number is (571) 272-8191. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronics Business Center (EBC) at 866-217-9197 (toll-free)

Sam Rizk, MSEE, ABD

Examiner

ART UNIT 2133

6/23/06

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